What Is Claimed Is:

1. An information processing system, comprising:

a host computer having a plurality of adapters;

a storage device having a plurality of host side ports connected to the host computer; a plurality of processors for controlling said plurality of host side ports; a cache memory, connected to said plurality of host side ports, for temporarily holding data in response to commands from said host computer; a shared memory for accumulating information relating to an internal composition of said storage device for reference by said plurality of processors; and an internal management device for outputting said compositional information to an external device; and

a management server connected respectively to said internal management device and said host computer, by a communications circuit;

wherein said host computer executes a path switching program, and establishes communications paths between said plurality of adapters and said plurality of host side ports;

wherein said storage device accumulates information relating to said communications paths, in said shared memory, and said internal management device refers to said information relating to communications paths and judges whether or not communications paths from said plurality of adapters to said cache memory can be secured in the event of at least one of said processors being blocked off; and

wherein, if a judgment result of said internal management device is that said communications paths can be secured, then said internal management device sends a notification indicating that it is possible to block off the processors for which said judgment was made, to said management server, via said communications circuit.

2. The information processing system according to claim 1, wherein said management server, after receiving said notification, sends information indicating that the communications paths connected to the processors for which said judgment has been made are to be blocked off, to said host computer executing said path switching program.

3. An information processing method for a host computer, a storage device, and a management server; the host computer including a plurality of adapters; the storage device having a plurality of host side ports connected to the host computer, a plurality of processors for controlling said plurality of host side ports, a cache memory connected to said plurality of host side ports for temporarily holding data in response to commands from said host computer; the management server connected respectively to said storage device and said host computer by a communications circuit; the information processing method comprising:

judging whether or not communications paths from said plurality of adapters to said cache memory can be secured in the event of at least one of said processors being blocked

off, based on information relating to communications paths from said plurality of adapters to said plurality of host side ports; and

sending a notification to said management server via said communications circuit, if it is judged that said communications paths can be secured, indicating that it is possible to block off the processor for which said judgment was made.

4. The information processing method of claim 3 further comprising receiving information indicating that the communications paths connected to the processors for which said judgment has been made are to be blocked off, from said management server, for executing a path switching program to establish communications paths between said plurality of adapters and said plurality of host side ports.

5. The information processing method of claim 3 further comprising accessing, from a shared memory of said storage device, information relating to communications paths between said plurality of adapters and said plurality of host side ports, said information to be used for judging whether or not communications paths from said plurality of adapters to said cache memory can be secured in the event of at least one of said processors being blocked off.